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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

In Re:	SARTSCHEV, Ronald A., et al.		
Serial No:	10/015865	Group:	
Filed:	12/12/01	Examiner:	
For:	COMPACT ATE WITH TIMESTAMP SYSTEM		

February 5, 2002

CERTIFICATE OF MAILING, EXPRESS MAIL, OR TRANSMISSION

I, Edmund J. Walsh, Reg. No. 32,950, certify that—

☑ this correspondence was placed in an envelope addressed to the Assistant Commissioner for Patents, Washington, DC 20231 and I have a reasonable basis to believe that it will be deposited with the US Postal Service as first class mail, postage prepaid, to the U.S. Patent and Trademark Office on or before February 5, 2002,

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Signature: Edmund J. Walsh Date: 2-5-02

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Sir/Madam:

In accordance with the duty of candor, the Applicant wishes to make of record the following documents listed on the attached form.

☑ A) This statement is being filed—

1. Within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
2. Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application;
3. Before the mailing of a first Office action on the merits; or
4. Before the mailing of a first Office action after the filing of a request for continued examination under § 1.114,

and therefore no additional fees are due,

OR

☐ B) This statement is being filed—

1. Before the mailing date of any of a final action under § 1.113, a notice of allowance under § 1.311, or an action that otherwise closes prosecution in the application; or
2. On or before payment of the issue fee,

and it is accompanied by one of:

☐ A fee set forth in § 1.17(p). The Commissioner is hereby authorized to charge **$180**, the payment of fees under § 1.17(p), to Deposit Account Number **20-0515**; or

☐ A statement specified in 37 C.F.R. 1.97 (e):

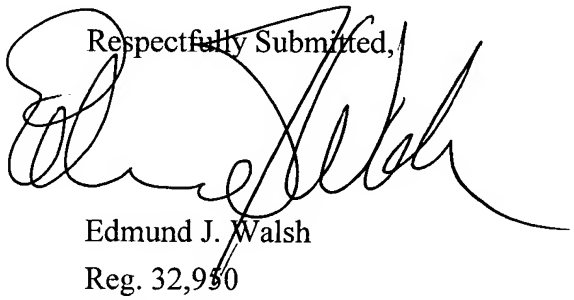
☐ Each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement; or

☐ No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information

disclosure statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the information disclosure statement.

This information disclosure statement is not to be construed as a representation that a search has been made, nor is it to be construed as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in § 1.56(b).

Respectfully Submitted,



Atty. Docket : 1490-US
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Edmund J. Walsh
Reg. 32,950
Attorney for Applicant

INFORMATION DISCLOSURE STATEMENT

Atty. Docket No. 1499	Serial No. 10/015865
Applicant: SARTSCHEV, Ronald A., et al.	
Filing Date: 12/12/01	Group:

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if appropriate
	AA	6,246,737	Jun 12, 2001	Kuglin	375	371	Oct 26, 1999
	AB	5,694,377	Dec 2, 1997	Kushnick	368	120	Apr 16, 1996
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	AE						
	AF						

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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AJ	Rainer Geiges, et al., "A High Resolution TDC Subsystem," IEEE Transactions on Nuclear Science, Vol. 41, No. 1, February 1, 1994
	AK	M. Sugawara, et al. "A 2.5V 100MS/s 8bit ADC Using Pre-Linearization Input Buffer and Level Up DAC/Subtractor," 1998 Symposium on VLSI Circuits Digest of Technical Papers, August 1998
	AL	J. Christiansen, "An Integrated CMOS 0.15 ns Digital Timing Generator for TDS's and Clock Distribution Systems," March 1995
	AM	Piotr Dudek, et al., "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," IEEE Transactions on Solid-State Circuits, Vol. 35, No. 2, February 2000
	AN	Yasuo Arai, et al., "A CMOS Four-Channel X 1K Time Memory LSI with 1-ns/b Resolution," IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, March 1992
	AO	Andrew E. Stevens, et al., "A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, December 1989

Examiner	Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT	Atty. Docket No. 1490	Serial No. 10/015865
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	AK	Keunoh Park, et al., "20ps Resolution Time-to-Digital Converter for Digital Storage Oscilloscopes," September 1999
	AL	Joonbae Park, et al., "An Auto-Ranging 50-210Mb/s Clock Recovery Circuit with a Time-to-Digital Converter," 1999 IEEE International Solid-State Circuits Conference, February 17, 1999
	AM	Elvi Raisanen-Ruotsalainen, et al., "An Integrated Time-to-Digital Converter with 30-ps Single-Shot Precision," IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000
	AN	R. Rankinen, et al., "Time-to-Digital Conversion with 10 ps Single Shot Resolution," 1991
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	AK	Hideki Shirasu, et al., "A VME 32 Channel Pipeline TDC Module with TMC LSIs," IEEE Transactions on Nuclear Science, Vol. 43, No. 3, June 1996
	AL	J. Kalisz, et al., "Time-to-Digital Converter with Direct Coding and 100ps Resolution," Electronics Letters, Vol. 31, No. 19, September 14, 1995
	AM	Dinis M. Santos, et al., "A CMOS Delay Locked Loop and Sub-Nanosecond Time-to-Digital Converter Chip," 1996
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	AJ	Timo Rahknone, et al., "Time Interval Measurements Using Integrated Tapped CMOS Delay Lines," 1990
	AK	P. Bailly, et al., "A 16-Channel Digital TDC Chip,"
	AL	Vadim Gutnik, et al., "On-Chip Picosecond Time Measurement," 2000 Symposium on VSLI Circuits Digest of Technical Papers, April 2000
	AM	Jozef Kalisz, et al., "Single-Chip Interpolating Time Counter With 200-ps Resolution and 43-s Range," IEEE Transactions on Instrumentation and Measurement, Vol. 46, No. 4, August 1997
	AN	C. Ljuslin, et al., "An Integrated 16-Channel CMOS Time to Digital Converter," IEEE Transactions on Nuclear Science, Vol. 41, No. 4, August 1994
	AO	Beomsup Kim, et al., "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2-um CMOS," IEEE Journal of Solid-State Circuits, Vol. 25, No. 6, December 1990

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	AK	"Using FastFrame Segmented Memory," Tektronix MBD: Applications, sysiyg://BODY.181/http://www.tektronix…easurement/App_Notes/dpo/fastframe/eng/
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